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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,989	11/09/2001	Han-Kun Hsieh	YUSO-131	1309

7590 12/02/2003

Raymond Sun
12420 Woodhall Way
Tustin, CA 92782

EXAMINER	
VU, DAVID	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,989	HSIEH ET AL.	
	Examiner	Art Unit	
	DAVID VU	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-3, 5-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al., (US 6,358,836) in view of Lin (US 6,348,399).

In re claims1-3, 5-8 and 10, Lu et al., in related text (Col. 8, Lines 9-60) and figures (Figs. 5A-5E), disclose a method of forming electroplated solder on an organic circuit board for making flip chip joints and board to board solder joints, comprising: providing an organic circuit board 12 (Col. 3, Lines 30-39) including a surface bearing electrical circuitry that includes at least one contact pad 74; a solder mask layer 78 that is placed on board surface and patterned to expose pad 74; a single thin metal layer (UBM) 96 that is deposited over board surface; a resist layer 100 with at least one opening located at pad 74 that is deposited over thin metal layer (UBM) 96; a solder material that is formed in opening by electroplating (Col. 8, Lines 53-60); resist layer and thin metal layer beneath resist layer being removed (Fig. 5E)

Lu et al., disclose all claimed subject matter, but fails to expressly disclose the method of forming UBM layer.

Lin, in related text, (Col. 3, Lines 4-8 and 16-20) discloses a thin metal layer (UBM) is deposited by CVD, PVD or PECVD method. It would have been obvious to one with ordinary skill in the art at the time of the invention to modify the Lu et al., by the method as taught by Lin since it becomes possible that the manufacture of a model chip scale package can be relatively simplified and economical, yield highly reliable.

2. Claims 4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al., (US 6,358,836) in view of Lin (US 6,348,399) and further in view of Akram (US 5,903,058).

Lu et al., disclose all claimed subject matter, but fails to expressly disclose the thickness of the UBM layer.

Akram, in related text, (Col. 6, Lines 5-11) discloses the thickness of the UBM layer may be about 3000Å. However, given the substantial Lu et al., in view of Lin and in further view of Akram, it would have been obvious to one with ordinary skill in the art at the time of the invention to judiciously adjust and control the thickness of the UBM layer through routine experimentation and optimization to achieve optimum benefits (see MPEP 2144.05) and it would not yield any unexpected results.

3. Claims 11-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al., (US 6,358,836) in view of Lin (US 6,348,399) and further in view of Sheridan et al., (US 6,489,229).

In re claims 11-14 and 16, Lu et al., in related text (Col. 8, Lines 9-60) and figures (Figs. 5A-5E), disclose a method of forming electroplated solder on an organic circuit board for

making flip chip joints and board to board solder joints, comprising: providing an organic circuit board 12 (Col. 3, Lines 30-39) including a surface bearing electrical circuitry that includes at least one contact pad 74; a solder mask layer 78 that is placed on board surface and patterned to expose pad 74; coating the surfaces of solder mask layer and pad with aqueous solutions which at least contains copper ions followed by reduction of copper ions, wherein there is no reduction of noble metal ions (See prior art reference USPAT 6,576,545{Col. 3, Lines. 15-29 and Col. 5, Lines 35-43} for evidence of the state of the art in which a electroless process involves coating the pad with aqueous solutions contains copper ions); a single thin metal layer (UBM) 96 that is deposited over board surface; a resist layer 100 with at least one opening located at pad 74 that is deposited over thin metal layer (UBM) 96; a solder material that is formed in opening by electroplating (Col. 8, Lines 53-60); resist layer and thin metal layer beneath resist layer being removed (Fig. 5E)

Lu et al., disclose all claimed subject matter, but fails to expressly disclose the method of forming UBM layer.

Lin, in related text, (Col. 3, Lines 4-8 and 16-20) discloses a thin metal layer (UBM) is deposited by electroless plating. It would have been obvious to one with ordinary skill in the art at the time of the invention to modify the Lu et al., by the method as taught by Lin since it becomes possible that the manufacture of a model chip scale package can be relatively simplified and economical, yield highly reliable.

Lu et al., disclose all claimed subject matter, but fails to expressly disclose the noble metal, such as gold, etc., should be avoided to be used as a part of the UBM layer.

Sheridan et al., in related text, (Col. 2, Lines 7-9) disclose a method for eliminating the Au layer formed on top of a Cu layer in a UBM stack. It would have been obvious to one with ordinary skill in the art at the time of the invention to modify the Lu et al., by the method as taught by Lin and Sheridan et al., since it becomes possible that the manufacture of a model chip scale package can be relatively simplified and economical. (See Sheridan et al., Col. 1, Lines 40-50).

4. Claims 17-21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al., (US 6,358,836) in view of Lin (US 6,348,399) and further in view of Sheridan et al., (US 6,489,229).

In re claims11-14, 16-21 and 23, Lu et al., in related text (Col. 2, Lines 5-64) and figures (Figs. 1A-1F), disclose a method of forming electroplated solder on an organic circuit board for making flip chip joints and board to board solder joints, comprising: providing an organic circuit board 12 (Col. 3, Lines 30-39) including a surface bearing electrical circuitry that includes at least one contact pad 14; a solder mask layer 24 that is placed on board surface 12 and patterned to expose pad 14; coating the surfaces of solder mask layer and pad with aqueous solutions which at least contains copper ions followed by reduction of copper ions, wherein there is no reduction of noble metal ions (See prior art reference USPAT 6,576,545{Col. 3, Lines. 15-29 and Col. 5, Lines 35-43} for evidence of the state of the art in which a electroless process involves coating the pad with aqueous solutions contains copper ions); a thin metal layer (UBM) 28/30 that is deposited over board surface 12; a resist layer 34 with at least one opening located at pad 14 that is deposited over thin metal layer (UBM) 28/30; a solder material

40 (Col. 8, Lines 52-58) that is formed in opening by electroplating (Col. 5, Lines 53-56); resist layer and thin metal layer beneath resist layer being removed (Figs. 1E-1F)

Lu et al., disclose all claimed subject matter, but fails to expressly disclose the method of forming UBM layer.

Lin, in related text, (Col. 3, Lines 4-8 and 16-20) discloses a thin metal layer (UBM) is deposited by electroless plating. It would have been obvious to one with ordinary skill in the art at the time of the invention to modify the Lu et al., by the method as taught by Lin since it becomes possible that the manufacture of a model chip scale package can be relatively simplified and economical, yield highly reliable.

Lu et al., disclose all claimed subject matter, but fails to expressly disclose the noble metal, such as gold, etc., should be avoided to be used as a part of the UBM layer.

Sheridan et al., in related text, (Col. 2, Lines 7-9) disclose a method for eliminating the Au layer formed on top of a Cu layer in a UBM stack. It would have been obvious to one with ordinary skill in the art at the time of the invention to modify the Lu et al., by the method as taught by Lin and Sheridan et al., since it becomes possible that the manufacture of a model chip scale package can be relatively simplified and economical. (See Sheridan et al., Col. 1, Lines 40-50).

5. Claims 15 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al., (US 6,358,836) in view of Lin (US 6,348,399) and further in view of Sheridan et al., (US 6,489,229) and Akram (US 5,903,058).

Lu et al., disclose all claimed subject matter, but fails to expressly disclose the thickness of the UBM layer.

Akram, in related text, (Col. 6, Lines 5-11) discloses the thickness of the UBM layer may be about 3000Å. However, given the substantial Lu et al., in view of Lin and in further view of Akram, it would have been obvious to one with ordinary skill in the art at the time of the invention to judiciously adjust and control the thickness of the UBM layer through routine experimentation and optimization to achieve optimum benefits (see MPEP 2144.05) and it would not yield any unexpected results.

Response to Arguments

6. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed 08/11/03 have been fully considered but they are not persuasive.

It is argued, at pages 6-7 of the remarks, that Lu et al., (US 6,358,836) fails to anticipate the present invention because Lu does not teach the process "applied to an organic circuit board". Lu et al., disclose a method of forming electroplated solder on an organic circuit board for making flip chip joints and board to board solder joints by providing an organic circuit board 12 (polyimide) (Col. 3, Lines 30-39). Moreover, the Applicant admitted Prior Art (AAPA) (US 2003/0022477) also teaches the substrate 106 is an organic circuit board (See [0004] and Figs. 1-2).

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is 703-305-0391. The examiner can normally be reached on Monday-Friday 8:00am-5: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

DV

David Vu.

David Nelms
Supervisory Patent Examiner
Technology Center 2800